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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,589	10/24/2003	Shelton Lu	JCLA11007	9478

7590 09/07/2004

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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,589	LU ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of Patterson et al. (US Patent 5,080,958).

Regarding to claim 1, figure 2 of Background of the Invention discloses an integrated circuit package substrate, at least comprising a plurality of patterned conductive layers 214 stacked over each other, wherein the outermost patterned conductive layer 214(a), 214(f) furthermore has a plurality of bonding pads 220a, 220b thereon; a plurality of dielectric layers 202 respectively sandwiched between a pair of neighboring patterned conductive layers 214, wherein at least one of the dielectric layers is an organic dielectric layer 202(b), 202(a), 202(d), 202(e); and a plurality of vias 218 respectively passing through at least one of the dielectric layer 202(a), 202(b), 202(d), 202(e) for connecting at least two of the patterned conductive layers 214 electrically.

Background of the Invention does not disclose at least one of the dielectric layer is a ceramic dielectric layer. However, Patterson et al. teach at least one of the dielectric layer is a ceramic dielectric layer as set forth in column 4, lines 50-60, and column 8, lines 7-27.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form at least one of the dielectric layer to be a ceramic dielectric layer, as taught by Patterson et al. in order to increase the density and complexity of the circuitry without significantly increasing the dimensions of the entire construct (col. 1, lines 24-27).

Regarding to claim 2, Background of the Invention discloses the IC package substrate wherein one of the dielectric layers is a dielectric core layer 202c.

Background of the Invention does not disclose the dielectric core layer is the ceramic dielectric layer. However, Patterson et al. teach the dielectric core layer is the ceramic dielectric layer (col. 4, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric core layer to be the ceramic dielectric layer, as taught by Patterson et al. in order to increase the density and complexity of the circuitry without significantly increasing the dimensions of the entire construct (col. 1, lines 24-27).

Regarding to claims 3 and 8, Background of the Invention discloses the IC package substrate wherein the dielectric layers are symmetrically distributed on each side of the dielectric core layer 132, 202c, 232c (figures 1-3).

Regarding to claims 4 and 9, Background of the Invention discloses the claimed invention except for the IC package substrate wherein the dielectric layers are non-symmetrically distributed on each side of the dielectric core layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the IC package substrate wherein the dielectric layers are non-symmetrically distributed on each side of the dielectric core layer, since it has been held that rearranging parts of an invention involves only routine skill in the art.

Regarding to claims 5 and 10, Background of the Invention in view of Patterson et al. disclose the claimed invention except for the IC package substrate wherein all the remaining dielectric layers are positioned on one side of the ceramic dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the IC package substrate wherein all the remaining dielectric layers are positioned on one side of the ceramic dielectric layer, since it has been held that rearranging parts of an invention involves only routine skill in the art.

Regarding to claim 6, figures 1 and 2 of Background of the Invention discloses a chip package structure, at least comprising an integrated circuit carrier having a first surface and a second surface, wherein the IC carrier at least having a plurality of patterned conductive layers 214 stacked over each other, wherein the patterned conductive layer 214(a) closest to the first surface furthermore has a plurality of bonding pads 220(a) thereon; a plurality of dielectric layers 202 respectively sandwiched between a pair of neighboring patterned conductive layer 214, wherein at least one of the dielectric layers 202(b), 202(a), 202(d), 202(e) is an organic dielectric layer; and a plurality of vias 218 passing through at least one of the dielectric layer 202(b) for connecting at least two of the patterned conductive layers 214(b) and 214(c) electrically; and a chip 120 attached to the first surface of the IC carrier and connected electrically to the IC carrier via the bonding pads (figures 1-3).

Background of the Invention does not disclose at least one of the dielectric layer is a ceramic dielectric layer. However, Patterson et al. teach at least one of the dielectric layer is a ceramic dielectric layer as set forth in column 4, lines 50-60, and column 8, lines 7-27.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form at least one of the dielectric layer to be a ceramic dielectric layer, as taught by Patterson et al. in order to increase the density and complexity of the circuitry without significantly increasing the dimensions of the entire construct (col. 1, lines 24-27).

Regarding to claim 7, figure 2 of Background of the Invention discloses the chip package structure wherein one of the dielectric layers is a dielectric core layer 202c.

Background of the Invention does not disclose the dielectric core layer is the ceramic dielectric layer. However, Patterson et al. teach the dielectric core layer is the ceramic dielectric layer (col. 4, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric core layer being the ceramic dielectric layer, as taught by Patterson et al. in order to enhance the rigidity of the package substrate.

Regarding to claim 11, Background of the Invention discloses the chip package structure wherein the chip is electrically connected to the IC carrier through a flip chip bonding or a wire bonding process (fig. 1).

Regarding to claim 12, Background of the Invention discloses the chip package structure wherein the package furthermore comprises a plurality of contacts 118, 222, 242 attached to the second surface of the IC carrier (figures 1-3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

09/02/04

Mai-Huong Tran
Examiner
Art Unit 2818